

### REMARKS

Claims 1-9, 11-16, 18-20, 38-45, and 47-50 are pending in the present application.

In the office action mailed June 6, 2005 (the "Office Action"), claims 11-15 were rejected under 35 U.S.C. 112, second paragraph. The Examiner further rejected claims 1-9, 16, 18-20, 38-41, and 47-50 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,060,355 to Batra *et al.* (the "Batra patent"). Claims 42-45 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Batra patent in view of U.S. Patent No. 5,340,765 to Dennison *et al.* (the "Dennison patent").

With respect to the rejection of claims 11-15 under 35 U.S.C. 112, second paragraph, claim 11 has been amended to use terms other than "smooth," "close proximity," and "near," as requested by the Examiner. Therefore, the rejections of claims 11-15 under 35 U.S.C. 112, second paragraph, should be withdrawn. It will be apparent from the amendments to claim 11, and the comments below, that the amendments were made independent of the cited references. None of previously mentioned amendments narrow or further limit the scope of the invention as recited by the respective claim. Generally, the amendments to claim 11 make explicit what is implicit in the claim, add language that is inherent in the unamended claim, or merely redefine a claim term that is previously apparent from the description in the specification. Consequently, the amendments should not be construed as being "narrowing amendments," because these amendments were not made for a substantial reason related to patentability.

As previously mentioned, claims 1-9, 16, 18-20, 38-41, and 47-50 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Batra patent. The Batra patent is directed to a process for forming a capacitor having a roughened surface. The process employs hemispherical grained ("HSG") silicon layers. An embodiment of a capacitor formed using the process is illustrated in Figure 6 of the Batra patent. A DRAM cell 85 includes a bottom electrode having a rough layer 86 formed over a substrate 50. The cell 85 is completed by forming a dielectric layer 90 and a top electrode 92 on the dielectric layer 90. *See* col. 6, lines 17-24. In contrast with the conventional process of forming memory cells having HSG, as described by the Batra patent, the inventive process incorporates a surface seeding method for forming a rough surface from a silicon-germanium layer. As shown in Figure 6, the resulting

capacitor structure for the cell 85 is surrounded by a BPSG structural layer 22 and only the dielectric layer 90 and the top electrode 92 extend beyond BPSG structural layer 22.

Claims 1, 6, 16, 38, and 47 are patentably distinct from the Batra patent because the Batra patent fails to disclose the combination of limitations recited by the respective claims. For example, with respect to claim 1, the Batra patent fails to disclose a semiconductor structure including a structure formed from a polycrystalline material including silicon-germanium alloy that has a portion extending beyond a nonconductive material, the portion having first and second surfaces and further including an electrode layer formed over at least a portion of the first and second surfaces of the portion of the structure extending beyond the nonconductive material. As previously discussed, the Batra patent discloses a structure having a HSG layer formed on a substrate 50 that is coextensive with the upper surface of the BPSG structural layer 22. As described in the Batra patent, the electrode that includes both the substrate 50 and the rough layer 86 is formed through a planarization step so that the electrodes of adjacent cells can be isolated. *See* col. 6, lines 19-21. In contrast, as recited in claim 1, a structure includes portions having first and second surfaces that extend beyond a layer of nonconductive material, and an electrode layer formed over portions of the first and second surfaces. The dielectric layer 90 and the top electrode 92 in the Batra patent are not formed over first and second surfaces of the electrode having the substrate 50 and the rough layer 86.

Claims 6, 16, 38, and 47 also recite limitations similar to claim 1 which the Batra patent fails to disclose. Claim 6 recites a capacitor including a dielectric, a bottom electrode coupled to the dielectric and having portions extending beyond a nonconductive material, the portions having first and second surfaces, and a top electrode formed adjoining the dielectric and covering at least a portion of the first and second surfaces of the portions of the bottom electrode that extend beyond the nonconductive material. Claim 16 recites a method for making a semiconductor structure including, among other things, forming a structure from a polycrystalline material including a silicon-germanium alloy having a portion extending beyond a nonconductive material, the portion having first and second surfaces, and further including forming an electrode layer over at least a portion of the first and second surfaces of the portion of the structure extending beyond the nonconductive material. Claim 38 recites a semiconductor structure including, among other things, a second layer formed from a silicon-germanium alloy

and formed abutting a second surface of a first layer, the second layer including portions extending beyond a non-conductive material, the portions extending beyond the non-conductive material having first and second surfaces, and further including a third layer formed over at least a portion of the first and second surfaces of the portions extending beyond the non-conductive material. Claim 48 recites a capacitor, in pertinent part, including a first electrode layer having first and second surfaces formed from undoped silicon, the first electrode layer having a U-shaped structure and the first surface corresponds to an inner surface and the second surface corresponds to an outer surface and further including a dielectric layer formed on a rough layer and on the second surface of the first electrode layer.

As previously discussed with respect to claim 1, the Batra patent does not disclose a semiconductor structure or capacitor having an electrode on which a rough surface is formed that extends beyond a layer of non-conductor material. As shown in Figure 6, the DRAM cell 85 includes an electrode including the substrate 50 and the rough layer 86 that does not extend beyond the BPSG structural layer 22. Additionally, the top electrode 92 and the dielectric layer 90 are not formed over at least a portion of first and second surfaces of the lower electrode.

For the foregoing reasons, claims 1, 6, 16, 38, and 47 are patentably distinct from the Batra patent. Claims 2-5, which depend from claim 1, claims 7-9, which depend from claim 6, claims 18-20, which depend from claims 16, claims 39-41, which depend from claim 38, and claims 48-50, which depend from claim 47, are similarly patentably distinct from the Batra patent based on their dependency from a respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. Therefore, the rejection of claims 1-9, 16, 18-20, 38-41, and 47-50 under 35 U.S.C. 102(e) should be withdrawn.

As previously mentioned, claims 42-45 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Batra patent in view of the Dennison patent.

The rejection of claims 42-45 under 35 U.S.C. 103(a) must be withdrawn because both the Batra patent, which as will be explained in more detail below, cannot be relied upon as prior art in supporting a rejection under 35 U.S.C. 103(a), in view of 35 U.S.C. 103(c). 35 U.S.C. 103(c) states:

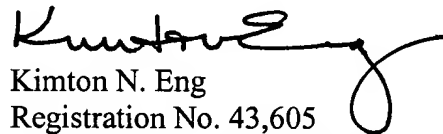
“(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under [section 103] where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.”

The Batra patent has been cited as a 35 U.S.C. 102(e) reference, as previously discussed. With respect to common ownership, both the Batra patent and the present application were, at the time the invention was made, owned by, or subject to an obligation of assignment to, the same person, namely, Micron Technology, Inc. The cover page of the Batra patent indicates that the Assignee is Micron Technology, Inc., and the assignment of the present application to the same entity is recorded at Reel/Frame number 012226/0547 on September 26, 2001.

Therefore, under 35 U.S.C. 103(c), the rejection of claims 42-45 under 35 U.S.C. 103(a) as being unpatentable over the Batra patent in view of the Dennison patent, cannot be maintained, and consequently, must be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,  
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Enclosures:

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